Solution based prompt inorganic condensation and atomic layer deposition of Al_2O_3 films: A side-by-side comparison

Sean W. Smith
School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, Oregon 97331-5501

Wei Wang and Douglas A. Keszler
Department of Chemistry, Oregon State University, Corvallis, Oregon 97331-4003

John F. Conley, Jr.[a)]
School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, Oregon 97331-5501

(Received 13 February 2014; accepted 22 April 2014; published 7 May 2014)

A comparison was made of Al_2O_3 films deposited on Si via prompt inorganic condensation (PIC) and atomic layer deposition (ALD). Current–voltage measurements as a function of annealing temperature indicate that the solution-processed PIC films, annealed at 500 °C, exhibit lower leakage and roughly equivalent breakdown strength in comparison to ALD films. PIC films are less dense than as-deposited ALD films and capacitance–voltage measurements indicate a lower relative dielectric constant. On the basis of x-ray photoelectron spectroscopy, transmission electron microscopy, and energy dispersive x-ray spectroscopy, it is found that the 500 °C anneal results in the formation of a ~6 nm thick interfacial SiO_2 layer at the Si interface. This SiO_2 interfacial layer significantly affects the electrical performance of PIC Al_2O_3 films deposited on Si. © *2014 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4874806]

I. INTRODUCTION

In this work, we compare the physical and electrical properties of Al_2O_3 films deposited on Si via atomic layer deposition (ALD) with those deposited via the solution route of prompt inorganic condensation (PIC), focusing on how process parameters affect properties. Since the study involves a mature technique (ALD) and an emerging method (PIC), it provides a unique baseline study for guiding future studies and development of the PIC method as well as other solution processing approaches.

ALD has become widely used for the synthesis of dense, planar thin films and highly conformal coatings on high topography substrates.[1,2] In terms of sustainable manufacturing, however, ALD suffers from slow deposition rates, low precursor utilization, and the requirement of a vacuum system. Solution based methods are an attractive alternative for planar applications, because they enable deposition at atmospheric pressure and with shorter processing times. Traditional solution based approaches, however, are often predicated on the use of metal-organic precursors. Efficient and complete conversion of these precursors to high-quality films is rarely achieved, as pyrolysis and high-temperature annealing are generally used to remove bulky organic ligands and densify the films.[3,4] The large volume change associated with ligand loss leads to high surface roughness and porosity.[5] In the alternative approach of PIC, precursor solutions containing nanosized inorganic clusters enable the deposition of dense, smooth, high-quality films with modest annealing temperatures.[6–8]

In this study, we focus primarily on the effects of varying postdeposition anneal temperatures on Al_2O_3 thin film properties and performance. Ellipsometry was used to measure the film thickness and optical properties. X-ray reflectivity (XRR) was used to measure film thickness, film density, and film roughness. $Al/Al_2O_3/Si$ MOS capacitors were used for current versus voltage (I-V) measurements to evaluate the leakage current and dominant charge transport mechanisms and capacitance versus voltage (C-V) measurements were used to assess the relative dielectric constant and estimate bulk and interfacial trap densities. Finally, x-ray photoelectron spectroscopy (XPS), energy dispersive x-ray spectroscopy (EDS), and transmission electron microscopy (TEM) were used to examine the Al_2O_3/Si interface. Collectively, these results provide an initial snapshot of the film and interface characteristics that govern the electrical performance of solution-processed Al_2O_3 films.

II. EXPERIMENT

All films were deposited on ⟨100⟩ Si coupons covered with 2 nm of native oxide. Lightly doped (10^{15}/cm^3 B) *p*-type Si was used for capacitance voltage testing while degenerately doped (10^{19}/cm^3 As) *n*-type Si was used for current voltage testing. The aqueous Al-based precursor used for PIC (described in Refs. 6–8) was prepared with Al concentrations between 0.1 and 0.3 M. To produce the hydrophilic surface required for successful deposition of the aqueous precursor, substrates were exposed to a 150 W O_2 plasma for 10 min immediately prior to PIC. It was determined that the O_2 plasma treatment resulted in a less than a 0.5 nm increase in the thickness of the native oxide. Target Al_2O_3 film thicknesses were 10, 30, or 100 nm. Films of 10 and 30 nm were deposited with a single coating. Thicker films of 100 nm were deposited with five sequential coatings. Postdeposition anneals were performed in air at temperatures

a)Electronic mail: jconley@eecs.oregonstate.edu

ranging from 300 °C to 800 °C for 1 h with 5 °C/min ramp rates. Although both PIC and ALD targeted a nominal thickness of 30 nm, it was found that PIC films shrink with annealing due to water loss and densification and have measured thicknesses lower than the target thickness. The measured thickness is used to normalize data. ALD of Al_2O_3 was performed in a Picosun Sunale R-150 flow-through, hot-wall reactor at 300 °C by using trimethylaluminum and water as reactants. Select ALD samples received a 500 °C postdeposition anneal in air.

Film thickness was measured using a J.A. Woollam VASE Ellipsometer. Film thickness, density, and roughness were assessed by XRR using a Rigaku Ultima. XPS depth profiles were collected on a ThermoScientific ESCALAB 250 system. Cross sectional TEM images and EDS line scans were collected on a FEI TITAN 80-200 TEM/STEM with ChemiSTEM technology.

To assess electrical characteristics, MOS test structures were fabricated by thermally evaporating aluminum through a shadow mask to produce circular contacts approximately 60, 85, and 145 μm in diameter. Precise areas were measured with an optical microscope. Current–voltage (I-V) sweeps and ramped breakdown measurements were made using an Agilent 4155C semiconductor parameter analyzer. A positive bias was applied to the Al top contact, and the current was monitored as the voltage was increased past breakdown. To investigate the impact of temperature on the dominant conduction mechanism, select devices were also measured using a Temptronic heated stage. Capacitance-voltage (C-V) measurements were made by using an Agilent E4980A precision LCR meter at 100 kHz, sweeping the device from depletion to accumulation and back. The relative dielectric constant was extracted from the line slope on a plot of accumulation capacitance versus contact area, assuming a single layer film. Flatband voltage was extracted using the method outlined by Schroder.[9]

III. RESULTS AND DISCUSSION

Normalized plots of capacitance density versus electric field for 100 nm thick as-deposited ALD and annealed PIC Al_2O_3 films are shown in Fig. 1(a). Relative dielectric constants (κ), extracted from the maximum capacitance (C_{max}), and flat band voltage (V_{FB}) shift are shown in Fig. 1(b) for 30 and 100 nm thick as-deposited ALD and annealed PIC Al_2O_3 films. The V_{FB} shift is the difference between the measured and ideal flat band voltage. In agreement with previous reports,[10] the as-deposited ALD films exhibit low hysteresis with $\kappa = 9.3$ for 100 nm thick films and $\kappa = 8.1$ for 30 nm thick films. The ALD films exhibit a flat band voltage shift of 0.8 V for the 30 nm films and 0.5 V for the 100 nm films, indicating negative trapped charge in the film or at the interface, as is commonly reported for Al_2O_3 films.[11] The 100 nm thick PIC films, annealed at 300 °C in air, exhibit large hysteresis and a higher C_{max} ($\kappa = 10.4$) than the ALD films, likely due to the presence of mobile H^+ associated with residual water and -OH. The 300 °C annealed PIC films exhibit a flat band voltage shift of −0.4 V for the 30 nm films

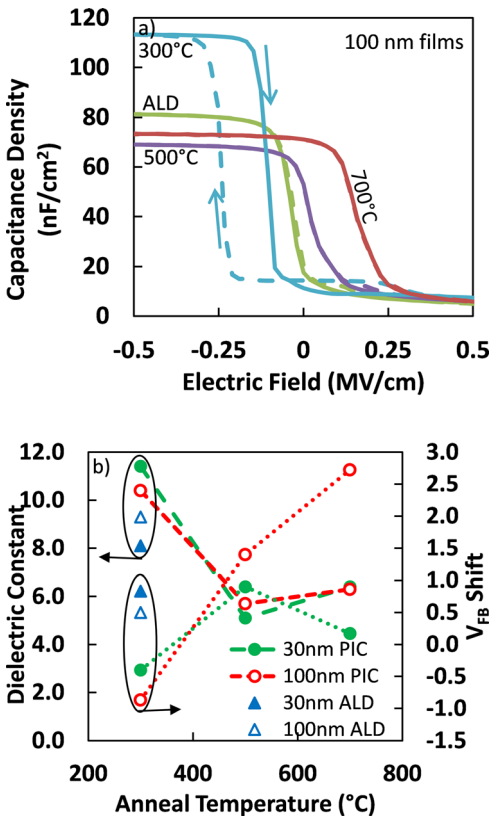

FIG. 1. (Color online) (a) Capacitance density vs electric field at 100 kHz and (b) extracted relative dielectric constant (κ) and flat band voltage shift (V_{FB}) vs temperature for annealed PIC and as-deposited ALD Al_2O_3 films.

and −0.9 V for the 100 nm thick films, indicating positive charge in the film or at the interface. Annealing at 500 °C eliminates hysteresis in the PIC films, reduces C_{max} ($\kappa = 5.7$), and shifts the V_{FB} to 0.9 V for the 30 nm and 1.4 V for the 100 nm films. The positive shift in the V_{FB} indicates either a reduction of positive charge and/or accumulation of negative charge at the interface or in the bulk of the film. The flat band voltages of the 500 °C annealed PIC films are shifted positively from ideal as was seen in the as-deposited ALD films and more typical of what is reported for Al_2O_3 films.[11] Annealing the PIC films at 700 °C leads to a slight increase in κ ($\kappa = 6.3$), further positive V_{FB} shift in the 100 nm films, but a negative V_{FB} shift in the 30 nm films. The different V_{FB} behavior could be due to relative influences of the bulk Al_2O_3 and interfacial SiO_2 layers. The decrease in both dielectric constant and hysteresis with increasing temperature are indicative of dehydration and densification of the PIC film.[12]

Table I lists density versus temperature for the nominally 30 nm thick as-deposited ALD and annealed PIC Al_2O_3 films. Density values were extracted from XRR measurements, modeled as a bilayer stack of Al_2O_3 on a 2 nm thick SiO_2 layer on silicon. It is seen that as-deposited PIC Al_2O_3 films are less dense than as-deposited ALD Al_2O_3. The density of the PIC films decreases with increasing anneal temperatures up to 350 °C. This decrease in PIC film density takes place in tandem with a reduction in dielectric constant and hysteresis (as seen in Fig. 1), which

TABLE I. Density of annealed PIC and as-deposited ALD Al_2O_3 thin films as measured by XRR (Ref. 12).

Film	Anneal temperature (°C)	Density (g/cm^3)
ALD	As deposited	3.23
PIC	250	2.58
	300	2.53
	350	2.41
	500	2.56
	700	2.77
	800	3.10

is attributed to the removal of water from the film.[12] Above 350 °C, densification of the PIC films takes place. Even at 800 °C, however, the density of PIC films is still below that of the as-deposited ALD films. The slight increase in κ between the 500 °C and 700 °C annealed PIC films is likely due to film densification. Consistent with their lower density than the ALD films, both the 500 °C and 700 °C annealed PIC films show significantly lower κ values than the ALD films.

Representative plots of leakage current density versus electric field and plots of the cumulative fraction of failed devices versus breakdown field are shown in Fig. 2 for 10 nm thick ALD and PIC Al_2O_3 films. The cumulative fraction plot is a way to visually display the natural variation present in breakdown field with a limited sample set. The

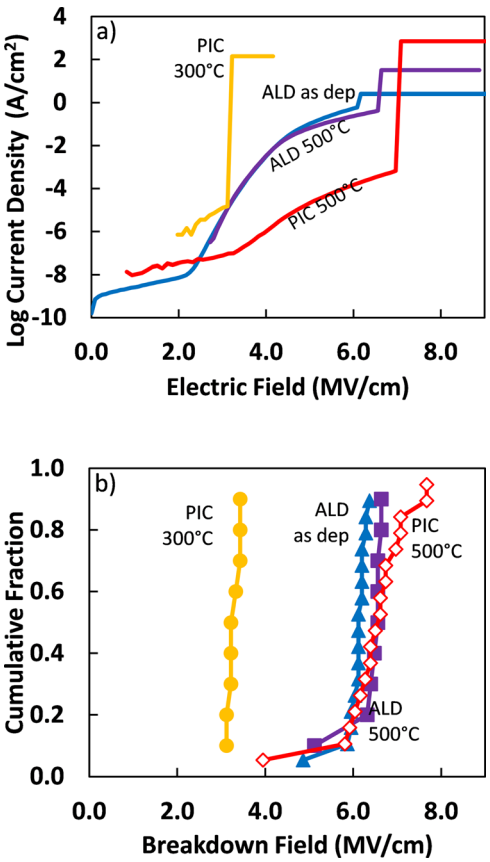

FIG. 2. (Color online) (a) Representative plots of current density vs electric field and (b) cumulative fraction plots of breakdown field for 10 nm thick PIC and ALD Al_2O_3 films with various annealing temperatures.

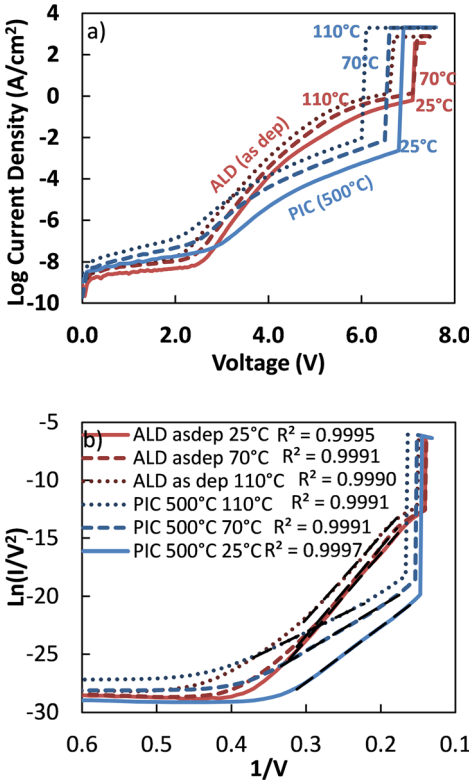

FIG. 3. (Color online) (a) Current voltage sweeps and (b) F-N plots of $\ln(I/V^2)$ vs 1/V for 10 nm thick as-deposited ALD and 500 °C annealed PIC Al_2O_3 films measured at 25 °C, 70 °C, 110 °C.

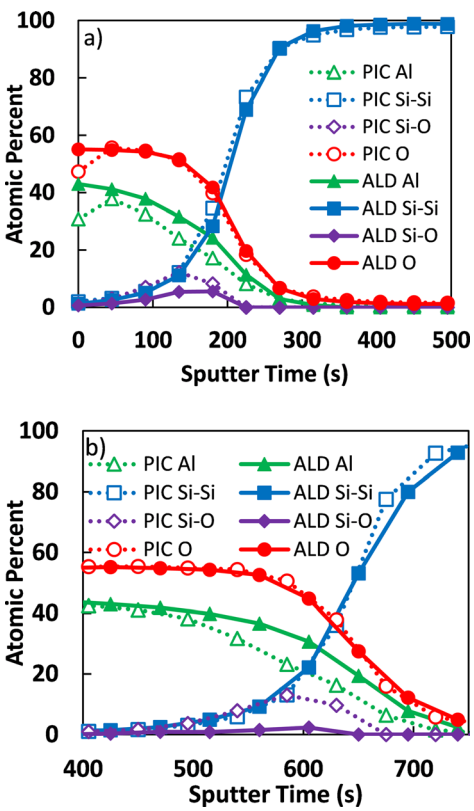

FIG. 4. (Color online) XPS sputter profiles for (a) 10 nm and (b) 30 nm Al_2O_3 films. Dotted lines/open symbols and solid lines/filled symbols represent 500 °C annealed PIC and as-deposited ALD films, respectively. Green triangles, purple diamonds, blue squares, and red circles represent Al, Si-O, Si-Si, and O, respectively.

as-deposited ALD films exhibit very low leakage currents at low fields (<2 MV/cm) with a nonlinear increase at higher fields, which is consistent with previous reports.[13] The I-V characteristics of the ALD films do not change significantly after a 500 °C anneal. As seen in Fig. 2(b), the as-deposited ALD films exhibit a narrow distribution of breakdown fields around roughly 6.1 MV/cm, which shifts slightly upward to about 6.3 MV/cm after the 500 °C anneal. The 300 °C annealed PIC films exhibit high leakage currents at low fields and modest breakdown strength (~3 MV/cm). In comparison to the ALD films, the 500 °C annealed PIC films exhibit similar low field (<2 MV/cm) leakage and breakdown strength, but lower high field (>3 MV/cm) leakage. The lower high field leakage of the PIC films is due to the higher electric field required for the onset of the high leakage "knee" combined with the lower slope of the postknee I-V curve. The superior leakage performance of the lower density 500 °C annealed PIC films compared to the higher density ALD films is unexpected, indicating that a MOS capacitor with a 500 °C annealed PIC film presents a higher barrier to electron transport than an MOS capacitor with an ALD Al_2O_3 film. This suggests that a wider bandgap (higher electron barrier) interfacial layer may be enhancing the leakage performance of the PIC films.

Representative plots of current versus voltage taken at 25, 70, and 110 °C for 10 nm thick as-deposited ALD or 500 °C annealed PIC Al_2O_3 films are shown in Fig. 3(a). At high electric fields, the current, I, due to quantum mechanical tunneling of electrons through a triangular barrier is described by the Fowler–Nordheim (F-N) equation as

$$I = \frac{q^2A^2}{8\pi h}\frac{V^2}{s^2\phi_0}\exp\left(-\frac{8\pi s(2m_0q)^{\frac{1}{2}}}{3h}\frac{\phi_0^{\frac{3}{2}}}{V}\right), \quad (1)$$

where q is the electronic charge, A is the device area, h is Planck's constant, V is the applied voltage, s is the thickness of the dielectric, φ_0 is the conduction band offset at the cathode, and m_0 is the effective mass of an electron. This relationship [Eq. (1)] can be linearized by plotting $\ln(I/V^2)$ versus 1/V, known as a F-N plot. The data from Fig. 3(a) show high linearity on the F-N plot in Fig. 3(b) with constant slopes for the ALD films[14] and temperature dependent slopes for the PIC films. Combined with the presence of the knee in all I-V curves, the good linear fits indicates a dominant role for tunneling in the ALD films and a strong *contributing* role for tunneling in the PIC films.[15,16] The lower slopes and higher turn-on voltage for tunneling exhibited by PIC films indicate that the PIC films present a higher tunnel barrier

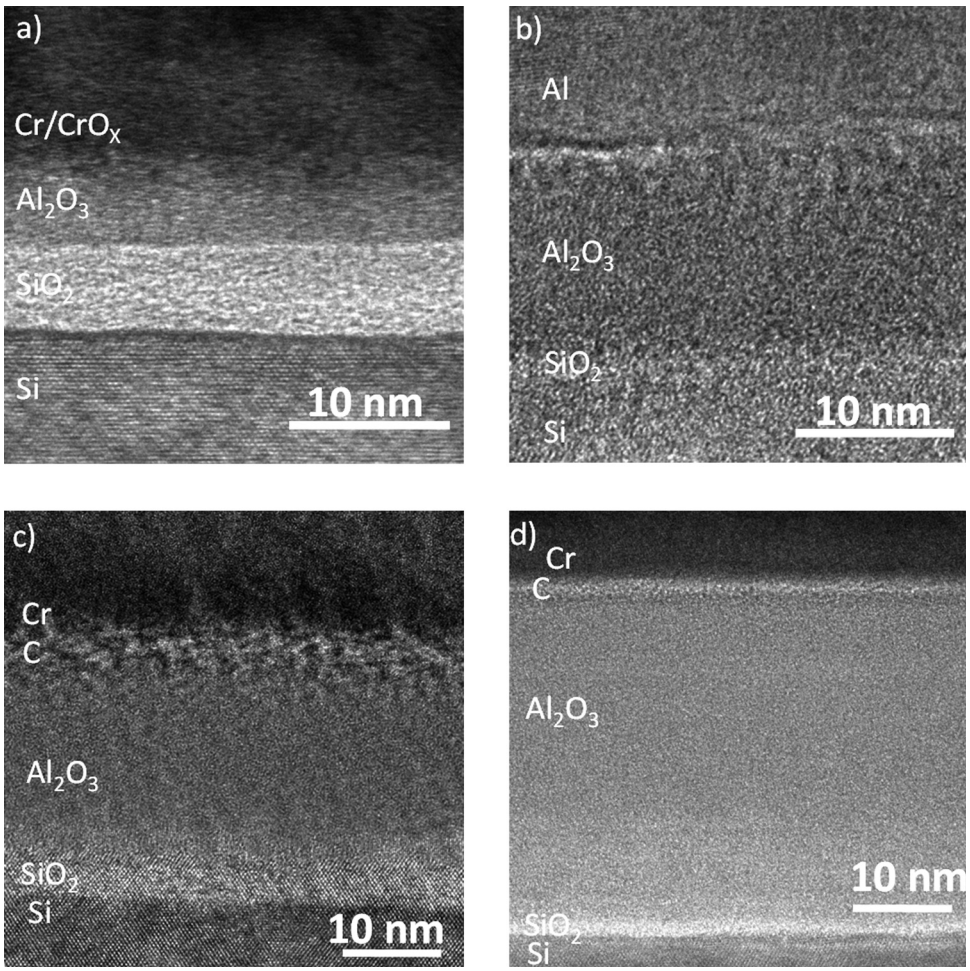

FIG. 5. Cross sectional TEM images of 10 nm thick (a) PIC and (b) ALD and 30 nm thick, (c) PIC and (d) ALD Al_2O_3 films on Si. ALD films were as-deposited while PIC films were annealed at 500 °C.

height than the ALD films, suggesting either a wider Al_2O_3 bandgap or the presence of a wide bandgap interfacial layer. The temperature dependence of the PIC films indicates the presence of multiple conduction mechanisms and suggests a contributing role for thermal conduction mechanisms such as Poole–Frenkel or Schottky emission. It was found that both ALD and PIC I-V data produced a poor fit to Poole–Frenkel and Schottky linearizations (not shown) over a broad voltage range. However, for the low voltage range (<3.5 V), excellent linearity was obtained, indicating that either Poole–Frenkel or Schottky play a strong role in conduction at low voltages before Fowler-Nordheim Tunneling increases at larger fields.

As seen from the preceding data, PIC films have smaller dielectric constants and lower densities than the ALD films, yet they exhibit smaller leakage currents in MOS capacitors. There must be an additional component of the MOS capacitor that is contributing to the performance. XPS sputter depth profiles of the Al, Si-Si, Si-O, and O signals in nominally 10 and 30 nm thick ALD and PIC Al_2O_3 films are shown in Fig. 4. The carbon profile was also collected but for both ALD and PIC films dropped to zero after the surface layer was sputtered away [clearly seen for the PIC film in (a)]. Zn was used in the production of PIC precursors; however, <0.3% Zn was detected throughout the PIC the films. For clarity, both the C and Zn profiles were omitted. The Si-O signal and Si-Si signals are based on the 103 eV Si2p peak and the 99.5 eV Si2p peak, respectively. The main difference between the two deposition methods is the Si-O profile. It is seen that the Si-O signal near the Si interface is more prominent in the PIC films (dashed purple line with open diamonds) than in the ALD films (solid purple line with filled diamonds), suggesting the presence of a thicker SiO_2 interfacial oxide layer in the PIC films than for the ALD films. Similar results are seen in both 10 and 30 nm films.

TEM images of nominally 10 and 30 nm thick of PIC ALD Al_2O_3 are shown in Fig. 5. The TEM images confirm the presence of an interfacial layer between the Al_2O_3 and the Si substrate for both ALD and PIC films. As seen in Fig. 5(a), the nominally 10 nm thick PIC film actually consists of a 5.4 nm layer of Al_2O_3 and a 5.9 nm thick interfacial layer, while the comparable ALD film in Fig. 5(b) consists of an 11.3 nm layer of Al_2O_3 with only a 1.8 nm thick interfacial layer. Similarly, the nominally 30 nm thick PIC film in Fig. 5(c) consists of 15.0 nm of Al_2O_3 with a 6.2 nm thick interfacial layer, while the comparable ALD film in Fig. 5(d) has 31.4 nm of Al_2O_3 and an approximately 2.1 nm thick interfacial layer. In both the nominally 10 and 30 nm thick PIC films, the interfacial layer was found to be approximately 6 nm thick, while for both ALD films the interfacial layer was only about 2 nm thick. The XPS profiles in Fig. 4 as well as the EDS line scans in Fig. 6 indicate that the interfacial layer is SiO_2.

EDS line scans of the samples used for the TEM images in Fig. 5 are shown in Fig. 6. The smaller distances in the figure correspond to the Si substrate, while the larger distances correspond to the Al_2O_3 film. Several differences between the PIC and ALD films are apparent. In the 10 nm films in Fig. 6(a), the PIC O signal relative to the PIC Al signal extends approximately 4 nm further toward the Si substrate, while the ALD O and ALD Al signals change in tandem toward the Si substrate. In addition, the PIC Si signal exhibits a shallower slope than the ALD Si signal between 15 and 20 nm [Fig. 6(a)]. Both of these observations are consistent with a thicker SiO_2 interfacial layer in the PIC film than in the ALD film. Similar results are seen in the 30 nm thick films in Fig. 6(b). Here, the PIC O signal extends approximately 7 nm further toward the substrate than the PIC Al signal, while the PIC Si signal plateaus across a width of 5 nm in this region, indicating a thick SiO_2 interfacial layer has formed. For the ALD films, the Al, Si, and O signals all change simultaneously at about 10 nm, indicating a thinner interfacial layer.

To account for the effects of the interfacial SiO_2 layer on MOS capacitor performance, the PIC and ALD films can be modeled as two capacitors in series. By using the thicknesses observed in TEM and assuming that the SiO_2 interfacial layer has a $\kappa = 3.9$, the κ value of Al_2O_3 in the 30 and 100 nm PIC films were calculated to be 5.8 and 5.9, respectively. These values are substantially smaller than the $\kappa = 8.7$ and $\kappa = 9.6$ observed for the 30 and 100 nm ALD

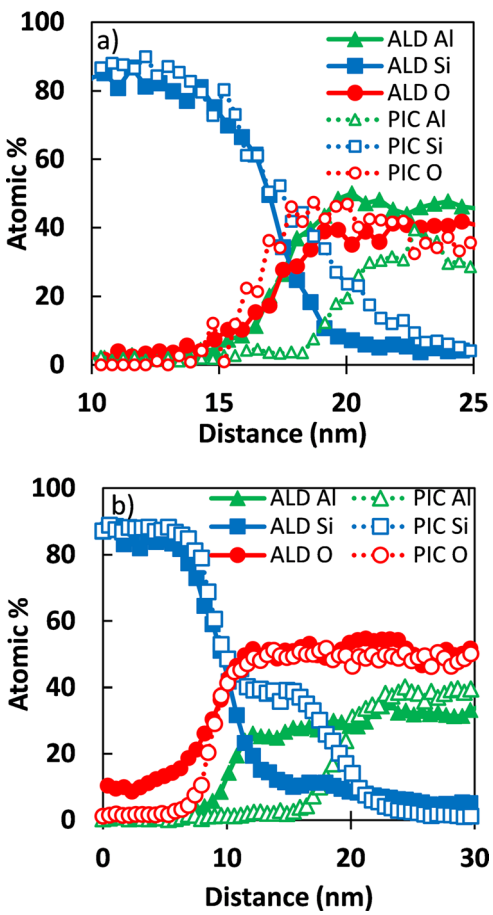

FIG. 6. (Color online) EDS line scan plots of atomic% aluminum (green triangles), silicon (blue squares), and oxygen (red circles) vs distance across the Si-Al_2O_3 film interface region for (a) 10 nm and (b) 30 nm Al_2O_3 films on Si. Dotted lines/open symbols and solid lines/filled symbols represent 500 °C annealed PIC and as-deposited ALD films, respectively.

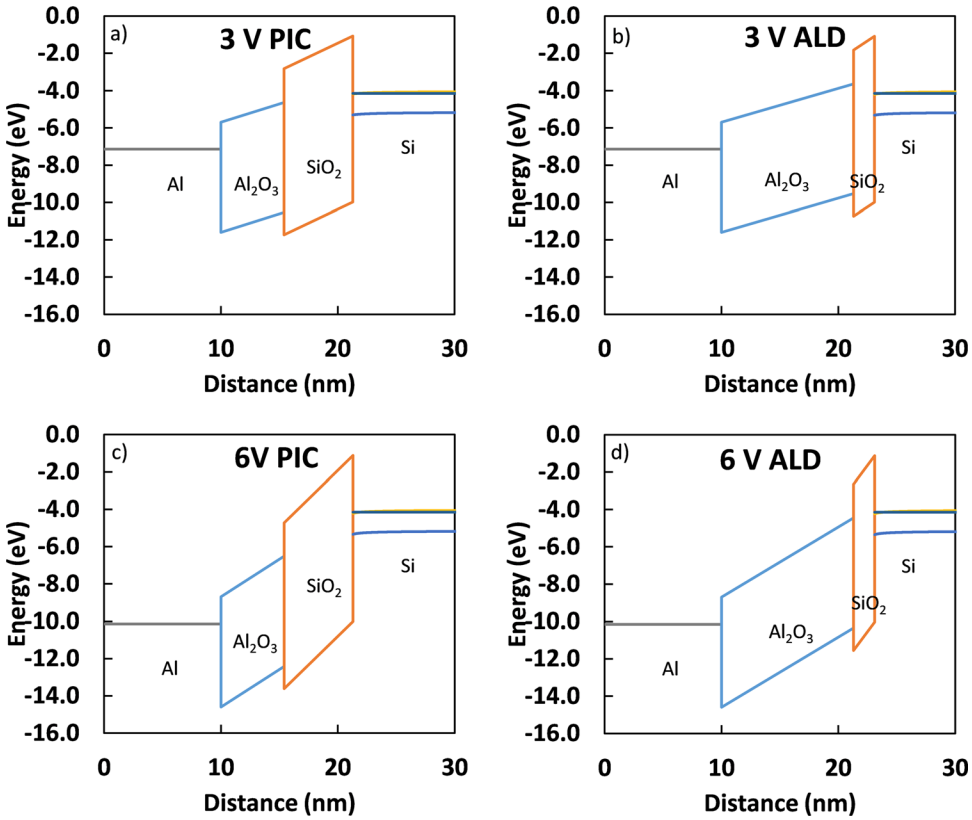

FIG. 7. (Color online) Proposed energy band diagrams for 10 nm thick (a), (c) PIC and (b), (d) ALD Al_2O_3 MOS devices with a bias of either (a), (b) 3 V or (c), (d) 6 V applied to the Al gate electrode.

films, respectively. These results indicate that both the PIC layer and the interfacial layer contribute to the lower κ observed in the MOS capacitors.

The thick SiO_2 interfacial layer accounts for the lower leakage currents as well as lower density and dielectric constant measured for the PIC films. MOS energy-band diagrams, simulated on the basis of the data in Figs. 2–6, for the nominally 10 nm thick PIC and ALD Al_2O_3 films are shown in Fig. 7. Biases of +3 V [Figs. 7(a) and 7(b)] and +6 V [Figs. 7(c) and 7(d)] applied to the Al electrode are considered.[17] The band diagrams confirm that the thick interfacial SiO_2 layer plays a dominant role in the PIC films, determining conduction under positive bias and providing an explanation for the seemingly contradictory electrical and structural behavior that was observed. It is clear that due to the difference in the relative thickness of the interfacial SiO_2 layers, a much larger portion of the potential drop occurs across the SiO_2 in the PIC films than in the ALD films.

Considering the +3 V bias simulations, which coincide with V_{ON} (the onset of the increased conduction slope) of the knee in the log(I)-V plot in both films [see Fig. 3(a)]. For the PIC device in Fig. 7(a), the Si conduction band edge (the conduction band in the degenerately doped n^+ Si substrate coincides with the Fermi level) is above the top of the Al_2O_3 conduction band so that electrons may tunnel directly through only the lower electron affinity SiO_2 layer, a situation known as step tunneling.[18] Because of the much thinner SiO_2 layer, the Si conduction band in the ALD device in Fig. 7(b) is below the top of the Al_2O_3 conduction band, so that electrons at the Fermi level in the Si must F-N tunnel into the conduction band of the Al_2O_3 layer. Comparing the band diagrams of the PIC device in Fig. 7(a) with the ALD device in Fig. 7(b), it is seen that at 3 V bias, the effective barrier for electron tunneling is lower for the ALD device than for the PIC device, accounting for the steeper initial log (J)-E slope for the ALD films than for the PIC films (Fig. 2).

Looking next at the +6 V bias simulations, it is seen that the Si conduction band for the PIC device [Fig. 7(c)] is now above the bottom of the SiO_2 conduction band on the anode side of the device so that F-N tunneling now may occur into the conduction band of the SiO_2 layer.[10] For the ALD device [Fig. 7(d)], because small voltage drop across the thinner SiO_2 layer, the Si conduction band is just above the top of the Al_2O_3 conduction band, so that step tunneling may occur through only the SiO_2 layer as the device approaches breakdown. The transition from F-N to direct tunneling through the SiO_2 layer coincides with a reduction in the log (J)-E slope in Fig. 2. It is likely, however, that the primary cause of the reduction in the log (J)-E slope is electron trapping in the Al_2O_3.

IV. SUMMARY AND CONCLUSIONS

The properties of Al_2O_3 films deposited on Si substrates via PIC and ALD have been evaluated, and the performance in MOS capacitors has been assessed. From electrical measurements, it was found that PIC films annealed at 300 °C exhibit large CV hysteresis, high leakage, and low breakdown strength, while annealing at 500 °C in air produced

lower leakage than ALD films of equivalent nominal physical thickness. From XRR measurements, it was found that the 500 °C annealed PIC films are less dense than as-deposited ALD films. From XPS, TEM, and EDS studies, it was found that annealing PIC films at 500 °C results in the formation of a thick interfacial SiO_2 layer which dominates electrical behavior. Simulated energy band diagrams of 500 °C annealed PIC and as-deposited ALD Al_2O_3 MOS devices are consistent with the trends in the electrical data and indicate that the SiO_2 interfacial layer dominates performance of the PIC Al_2O_3 films.

The results clearly demonstrate the aggressive chemical nature of aqueous-based metal nitrate solutions with respect to the oxidation of Si at modest temperatures. Such oxidation should be carefully considered and monitored in studies on solution-processed devices. The nature of interfacial oxide growth during PIC is the subject of ongoing work. Remarkably, the density of the PIC Al_2O_3 film does approach that of the ALD film, albeit at high temperatures. Considering the many processing parameters available for tuning the solution process, it maybe possible that high density PIC Al_2O_3 films can be realized at considerably lower temperatures.

ACKNOWLEDGMENTS

The authors thank Doug Tweet for a discussion about modeling XRR data, Steven Goelledge for assistance with the collection of XPS data at CAMCOR, Rose Ruther for her help in interpreting the XPS data, Peter Eschbach and Teresa Sawyer of the OSU Electron Microscopy Facility for assistance in the collection of TEM images, and Chris Tasker for equipment support, and the OSU Materials Synthesis and Characterization (MASC) Facility. Sean Smith and Wei Wang were supported by the NSF Center for Sustainable Materials Chemistry, grant number CHE-1102637. The TEM instrument used in this work was purchased through the National Science Foundation Major Research Instrumentation (MRI) Program under Grant No. 1040588 with matching funds from the Murdock Charitable Trust and the Oregon Nanoscience and Microtechnologies Institute (ONAMI).

[1]M. Leskelä and M. Ritala, Thin Solid Films **409**, 138 (2002).
[2]V. Miikkulainen, M. Leskelä, M. Ritala, and R. L. Puurunen, J. Appl. Phys. **113**, 021301 (2013).
[3]P. Vitanov, A. Harizanova, T. Ivanova, and T. Dimitrova, Thin Solid Films **517**, 6327 (2009).
[4]N. Özer, J. P. Cronin, Y. J. Yao, and A. P. Tomsia, Sol. Energy Mater. Sol. C **59**, 355 (1999).
[5]Y. Aoki, T. Kuniake, and A. Nakao, Chem. Mater. **17**, 450 (2005).
[6]K. Jiang, S. T. Meyers, M. D. Anderson, D. C. Johnson, and D. A. Keszler, Chem. Mater. **25**, 210 (2013).
[7]Z. L. Mesinger, J. T. Gatlin, S. T. Meyers, L. N. Zakharov, D. A. Keszler, and D. W. Johnson, Angew Chem. Int. Edit. **47**, 9484 (2008).
[8]W. Wang, K. M. Wents, S. E. Hayes, D. W. Johnson, and D. A. Keszler, Inorg. Chem. **50**, 4683 (2011).
[9]D. K. Schroeder, *Semiconductor Material and Device Characterization*, 3rd ed. (John Wiley & Sons, Hoboken, NJ, 2005), 328 pp.
[10]M. D. Groner, J. W. Elam, F. H. Fabreguette, and S. M. George, Thin Solid Films **413**, 186 (2002).
[11]R. S. Johnson, G. Lucovsky, and I. Baumvol, J. Vac. Sci. Technol. A **19**, 1353 (2001).
[12]W. Wang, "Synthesis and characterization of aluminum oxide based materials—From molecule to device," Ph.D. dissertation, Oregon State University, Corvallis, USA, 2013.
[13]F. Campabadal, J. M. Rafi, M. Zabala, O. Beldarrain, A. Faigon, H. Castan, A. Gomez, H. Garcia, and S. Duenas, J. Vac. Sci. Technol. B **29**, 01AA07 (2011).
[14]N. Alimardani, J. M. McGlone, J. F. Wager, and J. F. Conley, Jr., J. Vac. Sci. Technol. A **32**, 01A122-1 (2014).
[15]N. Alimardani, E. W. Cowell III, J. F. Wager, J. F. Conley, Jr., D. R. Evans, M. Chin, S. J. Kilpatrick, and M. Dubey, J. Vac. Sci. Technol. A **30**, 01A113 (2012).
[16]Y. Kim, S. Ohmi, K. Tsutsui, and H. Iwai, Jpn. J. Appl. Phys. **44**, 4032 (2005).
[17]R. G. Southwick III and W. B. Knowlton, IEEE Trans. Devices Mater. Rel. **6**, 136 (2006).
[18]N. Alimardani and J. F. Conley, Jr., Appl. Phys. Lett. **102**, 143501 (2013).